IN THE CLAIMS

Please amend the claims as follows:

Claims 1-24 (Canceled).

Claim 25 (New): A method for producing a chip-scale electronic package carried out at a substrate level, with a substrate including at least one chip having input/output pads on a substrate face as a front face, the method comprising:

a) forming, using a complex mould or stencil, an insulating stress relaxation layer on the front face, the relaxation layer covering the front face of the substrate with a relief surface that provides access wells to input/output pads and protruding parts configured to relax stresses, each protruding part having a tiered shape including at least one protuberant zone and at least one zone that is recessed relative to the protuberant zone, the recessed zone configured to support an electrical bonding pad;

b) forming electrically conductive tracks on the relaxation layer to connect input/output pads to the corresponding electrical bonding pads; and

c) forming electrical contacts with an exterior on the electrical bonding pads.

Claim 26 (New): A method according to claim 25, further comprising, between b) and c), forming an encapsulation layer on the relaxation layer with exposure of the electrical bonding pads.

Claim 27 (New): A method according to claim 25, in which, forming the stress relaxation layer using a mold comprises:

1) filling the mold with a given relaxation polymer or applying the polymer directly onto the front face of the substrate;

2) aligning the mold on the front face of the substrate;

3) pressing the mold on the front face of the substrate;

4) curing the polymer;

5) removing the mold.

Claim 28 (New): A method according to claim 25, in which, forming the stress relaxation layer using a stencil comprises:

1) applying the stencil to the front face of the substrate;

2) filling orifices in the stencil with a given relaxation polymer;

3) curing the polymer and separate the stencil from the substrate.

Claim 29 (New): A method according to claim 27, in which the given relaxation polymer is selected from amongst polyimide, BCB, or any other polymer capable of relieving stresses.

Claim 30 (New): A method according to claim 27, in which, after the stress relaxation layer is obtained on the front face of the substrate, polymer residues found on the input/output pads are removed.

Claim 31 (New): A method according to claim 25, in which the forming electrically conductive tracks comprises:

a) depositing a conductive material on the front face of the substrate covered with the relaxation layer;

b) separating rerouting lines and forming the electrical bonding pads by removal of conductive material located at the at least one protuberant zone of the protruding parts of the relaxation layer by mechanical lapping or by mechanical-chemical polishing.

Claim 32 (New): A method according to claim 25, in which the forming electrically conductive tracks is performed by chemical deposition of conductive material in access wells for input/output pads and in zones that are recessed in relation to the at least one protuberant zone of the protruding parts of the relaxation layer.

Claim 33 (New): A method according to claim 32, in which the conductive material is a metal.

Claim 34 (New): A method according to claim 25, in which the forming electrically conductive tracks comprises:

a) depositing a conductive material on the front face of the substrate covered with the relaxation layer;

b) lithography;

c) chemical etching;

d) stripping.

Claim 35 (New): A method according to claim 31, in which the depositing conductive material involves metallization.

Claim 36 (New): A method according to claim 25, in which the forming electrically conductive tracks comprises:

a) lithographic metallization of the front face of the substrate covered with the relaxation layer,

b) electrolysis;

c) stripping;

d) chemical etching.

Claim 37 (New): A method according to claim 26, in which the forming the encapsulation layer comprises:

a) depositing a layer of polymer over the entire front face of the substrate covered with the relaxation layer,

b) levelling the front face of the substrate;

c) exposing the electrical bonding pads.

Claim 38 (New): A method according to claim 26, in which the forming the encapsulation layer comprises:

a) levelling the front face of the substrate;

b) filling the access wells and recessed zones in the front face of the substrate with a thick polymer layer;

c) exposing the electrical bonding pads.

Claim 39 (New): A method according to claim 25, in which the electrical contacts with the exterior on the electrical bonding pads comprise fusible balls.

Claim 40 (New): A method according to claim 39, in which the fusible balls are introduced onto the electrical bonding pads using a technique selected from electrolysis of a fusible alloy, screen-printing of solder paste, and ball transfer.

Claim 41 (New): A method according to claim 25, in which the electrical contacts with the exterior on the electrical bonding pads are selected from amongst anisotropic conductive films and adhesives.

Claim 42 (New): A method according to claim 25, further comprising d) separating electronic chip-scale packages created at the substrate level.

Claim 43 (New): A method according to claim 25, in which, before or after the forming of the electrical contacts with the exterior on the electrical bonding pads, the rear face of the substrate is made thinner by lapping, mechanical-chemical polishing, or any other technique.

Claim 44 (New): A method according to claim 25, further comprising:

a) creating slots in the rear face of the substrate until the metallic layers represented by the integrated circuit input-output pads or by electrically conductive tracks are reached;

b) depositing, possibly localized, a metallic layer on the rear face of the substrate;

c) removing the metallization located on the surface of the rear face of the substrate.

Claim 45 (New): A complex mold or stencil configured to create a chip-scale package using the method described in claim 25.

Claim 46 (New): A complex mold or stencil according to claim 45, which is made using at least one technique from amongst wet or dry etching, electroforming, adhesion of plural pierced or un-pierced polymer films, molding, laser etching.

Claim 47 (New): A complex mold or stencil according to claim 45, which is made from silicon, metal, polymer.

Claim 48 (New): A chip-scale package manufactured at the substrate level created using the method according to claim 25.